AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

10. (Currently amended) ~~A system for data conversion~~A hardware architecture for a core of a processor, comprising:

~~a processor having~~ at least one unit for executing one of a logical or arithmetic operation; and

an object-oriented data conversion unit for recognizing a type of an object and an object address, for external data, the data conversion unit being arranged to precede the unit for executing a logical or arithmetic operation, whereby the data conversion unit recognizes ~~said~~a type of an object based upon a type of information accompanying the object address and matches the type of an object and the object address before one of an operation is performed or a predetermined type of object is generated in the event of non-match.

11. (Currently amended) The ~~system~~hardware architecture according to claim 10, wherein a memory location for the object address and a memory location of a register is respectively divided into a first area and a second area, whereby a type of the object is deposited in the first area.

12. (Currently amended) The ~~system~~ hardware architectureaccording to claim 10, whrein the object-oriented data conversion unit is arranged to follow the unit executing a logical or an arithmetic operation.

13. (Currently amended) The ~~system~~hardware architecture according to claim 10, wherein the object-oriented data conversion unit is arranged to precede the storing of the object in an external storage and a register file.

14. (Currently amended) The ~~system~~hardware architecture according to claim 10, wherein a register file is divided into a memory area for data and a memory area for a respective type indication of the data.

15. (Currently amended) The ~~system~~hardware architecture according to claim 10, further comprising a reduced instruction set processor.

16. (Currently amended) The ~~system~~hardware architecture according to claim 10, further comprising a complex instruction set processor.

17. (Previsously presented) A method for data conversion in a processor having at least one unit, the method comprising the steps of:

executing a logical or arithmetic operation in the processor;

implementing an object-oriented data conversion by a type information in an object address and by a type information of an object; and

generating an inequality of the objects to be operated by the logical or arithmetic operation based upon the type of objects matched to one another or a predetermined object type of an object.

18. (Previously presented) The method according to claim 17, further comprising the steps of:

dividing a memory location for an object address and a memory location of a register into a first and second area and a type information of the memory address deposited in the second area of the object address; and

noting the data of the register deposited in the second area in the first area.

19. (Previously presented) The method according to claim 17, wherein the processor includes a reduced instruction set processor.

20. (Previously presented) The method according to claim 17, wherein the processor includes a complex instruction set processor.